REMARKS

Claims 1-4 remain pending in the application. Favorable reconsideration is respectfully requested in view of the following remarks.

Claims 1, 2, and 3 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent Number 4,419,724 to Branigin et al. ("Branigin") in view of U.S. Patent Number 4,535,404 to Shenk ("Shenk"). This rejection is respectfully traversed.

To see why this ground of rejection should be withdrawn, it is informative to look precisely at what is taught in the Branigin and Shenk references. In its introductory paragraphs (Background section), Branigin acknowledges a prior art system in which units (modules) connected to a bus each include a lock register with a stage corresponding to each of the other units. When a master unit requests a function, it sends an address signal corresponding to the required slave unit and sends a lock signal to all the other units, thereby preventing communication between any unit other than the master and slave. The invention in Branigin is an extension of that prior art, permitting communication between more than one pair of units at a time.

On a more detailed consideration (such as in the passage extending from column 1, line 58 to column 2, line 16) Branigin teaches a system in which a priority controller receives transaction requests from one or more of the units. It allocates priority to the requests and responds by generating a grant ID signal corresponding to the highest priority requesting unit. Each unit contains a comparator for comparing the grant ID with its own ID. The requesting unit whose own ID matches the grant ID then becomes the source unit for that particular transaction and is thereby permitted access to the bus to send data over it. The data contains a lock bit and a destination ID identifying a destination unit. Each unit compares its own ID with the received destination ID and generates an acknowledge signal if there is a match. The acknowledge signal is sent over the bus to all units, which are responsive to the acknowledge signal, the grant ID, the destination ID and the lock bit to set/reset the register corresponding to the source and destination units.

As further described in Branigin (column 2, lines 31 to 45) each unit includes a bus interface MBIP, for applying a bus request to the priority controller, and a selector connected to the lock register. The selector receives information as to the availability of the intended destination unit and can prevent access to the bus if the intended destination unit is not available (see also column 5, lines 17-22 as noted by the Office). More specifically, (see column 7, lines 42-63) decoders in each unit produce output signals indicating the identity of

a source unit and a destination unit with which other units on the bus should not attempt to communicate. In the case where a requesting unit wants to communicate with a destination unit that is not available, as determined by the lock status of its corresponding bit in the lock registers of all the units, the requesting unit's interface MBIP does not send the request to the priority controller (as per column 8, lines 17-40).

As correctly acknowledged by the Office, Branigin does not disclose or suggest replacing the use of device IDs with memory mapping, as defined by Applicant's independent claim 1. The Office also acknowledges that Branigin does not disclose or suggest claim 1's defining the "target module having an address range in the memory map which address range includes the target address data."

This is not the full extent to which Branigin is deficient at disclosing Applicant's claimed subject matter because Applicant's claim 1 requires (and Branigan lacks) the further feature that the "decoding means ... decod[es] the target address data to produce module identity data relating to a target module, the target module having an address range in the memory map which address range includes the target address data."

The Office relies on the Shenk patent as making up for the deficiencies of Branigin, but this reliance is unfounded. Shenk describes a system which uses memory mapping for communicating between a processor and a number of peripheral devices, which the Office appears to equate with the modules of the present invention. According to Shenk, a computer is connected over a network to a cluster of display devices so that information can be displayed in each display device. It would seem inevitable that the same information will be displayed on each display device. Nevertheless, Shenk discusses the generality of transferring data between a processor and addresses within a peripheral controller by treating the peripheral controller as a memory space (see column 2, lines 17-24). The Office Action refers to column 1, lines 25-28 and 51-52 as a signpost indicating that Shenk discloses memory mapping, but it is respectfully submitted that Shenk does not go far enough to make Applicant's claims obvious.

As explained above, claim 1 requires all of the following features, which are absent from Branigin:

(i) "each module being assigned an address range in the memory map"; and

(ii) "each module comprising ... decoding means for ..."

(a) "... decoding the target address data to produce module identity data relating to a target module ..."

(b) "... the target module having an address range in the memory map which address range includes the target address data."

Shenk fails to disclose these missing features. First, there is no specific reference in Shenk to each of the modules being assigned an address range. However, even if one were to assume that it is implicit in memory mapping systems that peripheral devices are each allocated an address range as opposed to a unique address specific to the device, Shenk does not provide sufficient information to determine whether or not the address decoder mentioned in column 5, lines 21-68 operates in such a way as to render feature (ii)(a) obvious. In describing Figure 3, Shenk merely states that a processor 231, seeking to transfer data to/from a display controller, places a predetermined memory address on an address bus 304. Address decode logic 306 then "decodes" the predetermined address and initiates data transfer via interface control logic 316, which communicates with control logic 346 of the display controller. It is respectfully contended that this is simply not enough to give one of ordinary skill in the art sufficient motivation or incentive to consider modifying Branigin with the two features of assigning a memory range to each module and using a decoder to identify the module containing the target address.

Shenk discloses a means of attaching a peripheral device to a microprocessor's memory space, as opposed to its I/O space. This was the conventional approach at the time that the Shenk invention was conceived. Shenk actually describes a mechanism to allow the microprocessor memory interface to be attached to peripheral devices instead of just memory. A considerable number of modifications are needed for this to work. In the years since the inception of the Shenk invention it has become common to connect both memory and peripheral devices to the memory space of processors. In concert with this, their interface designs have been shaped with this in mind to such an extent that much of what is taught in Shenk is made obsolete by the now common bus systems such as PCI.

Applicant's invention differs in a number of technically significant ways:

- First, in Applicant's invention there are multiple initiators, which are often processors but could perhaps be other agents that can access a shared set of peripherals;
- Second, Applicant's bus must be arbitrated between the numerous initiators; and

- Third, Applicant's address decoding of individual memory and peripheral targets is placed on the processor side of the bus and not in the targets themselves.

Figure 3 of Shenk makes these distinctions clear. As a consequence, regardless of any considerations as to whether or not peripherals are assigned address ranges, Shenk does not in any case disclose or teach Applicant's invention for the reasons just set out.

In conclusion, it is respectfully submitted that Shenk and Branigin do not in fact meet the terms of Applicant's claims and their teaching, singly or in combination, does not render Applicant's claims obvious. It is submitted that Shenk does not provide the features "missing" from Branigin and, moreover, that there is no suggestion or teaching in either of the documents to motivate the person of ordinary skill in the art to consider modifying Branigin using the teaching in Shenk. Even if the person were so tempted, Shenk nevertheless still does not provide all of the missing elements defined by Applicant's claims and would leave the person of ordinary skill in the art with the task of undertaking further invention for himself in order to arrive at the concept currently encapsulated in the present claims.

Claims 2 and 3 each depend from claim 1, and are therefore patentable over any combination of Branigin and Shenk for at least the reasons set forth above.

In view of the foregoing, it is respectfully requested that the rejection of claims 1-3 under 35 U.S.C. §103(a) be withdrawn.

Claim 4 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Blum [sic: Branigan and Shenk – see numbered paragraph 7 of the Office Action] in view of U.S. Patent Number 5,761,516 to Rostoker et al. ("Rostoker"). This rejection is respectfully traversed.

Claim 4 depends from claim 1, and is therefore patentably distinguishable over the Branigan and Shenk patents for at least the same reasons as set forth above. The Rostoker patent fails to make up for the deficiencies of Branigin and Shenk because it, too, fails to disclose or even suggest the combination of features defined by claim 1. Accordingly, claim 4 is patentably distinguishable over the Branigan, Shenk and Rostoker patents regardless of whether these documents are considered individually or in combination. It is therefore respectfully requested that the rejection of claim 4 under 35 U.S.C. §103(a) be withdrawn.

The application is believed to be in condition for allowance. Prompt notice of same is respectfully requested.

Respectfully submitted,

Potomac Patent Group PLLC

Date: July 11, 2006

By: _____

Kenneth B. Leffler
Registration No. 36,075

P.O. Box 270
Fredericksburg, Virginia 22404
703-718-8884